UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/650,195	08/29/2000	Feng-Jong Edward Yang	F0255	8593

26615 7590 10/03/2003

HARRITY & SNYDER, LLP
11240 WAPLES MILL ROAD
SUITE 300
FAIRFAX, VA 22030

EXAMINER	
BATES, KEVIN T	
ART UNIT	PAPER NUMBER
2155	5

DATE MAILED: 10/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/650,195	YANG ET AL.	
	Examiner	Art Unit	
	Kevin Bates	2155	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 4, 5, 6, 9, 10, 11, 13, 14, 15, 16, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Runaldue (6,052,751) in view of Scheuneman (4,652,993)

Regarding claim 1, Runaldue discloses a network switch configured to control communication of data frames between stations (Column 4, lines 14 – 16), comprising: a plurality of receive devices corresponding to ports on the network switch (Column 2, lines 10 – 11), the receive devices configured to receive data frames from the stations (Column 4, lines 16 – 21); and an external memory interface configured to receive data from the plurality of receive devices (Column 2, lines 11 – 13), Runaldue does not explicitly indicate that the switch transfers a portion of the data received from a first one of the receive devices to a first memory, and transfer a portion of the data received from a second one of the receive devices to a second memory. Scheuneman teaches a means of high performance storage for memory. In this teaching he discloses that the switch transfers a portion of the data received from a first one of the receive devices to a first memory, and transfer a portion of the data received from a second one of the receive devices to a second memory (Figure 1a, element 1a to 3a and 1b to 3b and

Column 17, lines 60 – 64). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include Scheuneman's high performance storage in Runaldue's network switch in order to simultaneously move large amount of data or data frames (Column 2, lines 50 – 53).

Regarding claim 2, Runaldue discloses a scheduler coupled to the receive devices and configured to enable the received data frames to be outputted, which selects data to output (Column 5, lines 42 – 44). Runaldue does not explicitly mention that the scheduler simultaneously outputting first and second selection signals for outputting data from the first receive device and the second receive device, respectively. Scheuneman teaches a means of high performance storage for memory. In this teaching he discloses that the switch transfers a portion of the data received from a first one of the receive devices to a first memory, while you can transfer a portion of the data received from a second one of the receive devices to a second memory (Figure 1a, element 1a to 3a and 1b to 3b and Column 17, lines 60 – 64). Using Scheuneman's teaching, one could make an improvement to the scheduler in order for the scheduler to signal both data frames to move simultaneously. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include Scheuneman's high performance storage in Runaldue's network switch in order to improve Runaldue's scheduler to signal simultaneous data or data frames (Column 2, lines 50 – 53).

Regarding claim 4, as part of Scheuneman's high performance storage the external memory interface is further configured to simultaneously transfer the portions of

the data from the first and second receive devices to the first and second memories (Column 18, lines 29 – 31).

Regarding claim 5, as part of Scheuneman's high performance storage the external memory interface includes a first external memory bus and a second external memory bus, and the external memory interface is configured to simultaneously transfer data received from a first one of a first group of the receive devices via the first external memory bus and a second one of a second group of the receive devices via the second external memory bus (Column 45, lines 5 – 11).

Regarding claim 6, as part of Scheuneman's high performance storage the external memory interface is further configured to alternately transfer data received from the first group of receive devices to the first and second memories and to alternately transfer data received from the second group of receive devices to the first and second memories because as seen in figure 1a, the first device, 1a, goes through the multiplexer 2a and can send to any memory unit and the second device, 1b, goes through the multiplexer 2b and can travel to any storage unit, so the interface is configured to transfer data to the first or second memory unit for each device.

Regarding claim 10, Runaldue discloses a network switch that controls communication of data frames between stations (Column 4, lines 14 – 16), a method of storing data frame information, comprising: receiving a plurality of data frames (Column 4, lines 16 – 21); temporarily storing the received data frames (Column 6, lines 54 – 56); but Runaldue does not explicitly disclose simultaneously transferring data frame information to at least a first memory and a second memory. Scheuneman teaches a

means of high performance storage for memory. In this teaching he discloses that the switch transfers a portion of the data received from a first one of the receive devices to a first memory, and transfer a portion of the data received from a second one of the receive devices to a second memory (Figure 1a, element 1a to 3a and 1b to 3b and Column 17, lines 60 – 64). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include Scheuneman's high performance storage in Runaldue's network switch in order to simultaneously move large amount of data or data frames (Column 2, lines 50 – 53).

Regarding claim 11, Runaldue discloses selection signals to first and second receive devices for selectively outputting data stored in the first and second receive devices (Column 5, lines 42 – 44). Runaldue does not explicitly mention that the first and second receive devices transmit simultaneously. Scheuneman teaches a means of high performance storage for memory. In this teaching he discloses that the switch transfers a portion of the data received from a first one of the receive devices to a first memory, while you can transfer a portion of the data received from a second one of the receive devices to a second memory (Figure 1a, element 1a to 3a and 1b to 3b and Column 17, lines 60 – 64). Using Scheuneman's teaching, one could make an improvement to be able to send data frames simultaneously. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include Scheuneman's high performance storage in Runaldue's network switch in order to improve performance by simultaneously transfering data or data frames (Column 2, lines 50 – 53).

Regarding claims 9 and 15, as part of Scheuneman's high performance storage the external memory interface is further configured to simultaneously retrieve data from the first and second memories (Column 18, lines 29 – 31).

Regarding claim 14, as part of Scheuneman's high performance storage the data frames are temporarily stored in a plurality of receive devices, further comprising: alternately transferring data frame information from a first group of the receive devices to the first and second memories; and alternately transferring data frame information from a second group of the receive devices to the first and second memories because as seen in figure 1a, the first device, 1a, goes through the multiplexer 2a and can send to any memory unit and the second device, 1b, goes through the multiplexer 2b and can travel to any storage unit, so the interface is configured to transfer data to the first or second memory unit for each device.

Regarding claim 13, as part of Scheuneman's high performance storage the simultaneously transferring includes: sending a portion of a first data frame via a first external memory bus and sending a portion of a second data frame via a second external memory bus (Column 45, lines 5 – 11).

Regarding claim 16, Runaldue discloses a data communication system for controlling the communication of data frames between stations, comprising: a plurality of receive devices configured to receive data frames from the stations (Column 4, lines 14 - 16); a scheduler coupled to the plurality of receive devices and configured to generate selection signals to selectively output data frame information from the receive devices (Column 5, lines 42 – 44); and a switching device configured to receive the data

frame information (Column 2, lines 11 – 13). Runaldue does not explicitly indicate that the communication system simultaneously transfers data frame information from a first one of the data frames via a first external memory bus and data frame information from a second one of the data frames via a second external memory bus. Scheuneman teaches a high performance storage which includes an external memory interface with a first external memory bus and a second external memory bus, and the external memory interface is configured to simultaneously transfer data received from a first one of a first group of the receive devices via the first external memory bus and a second one of a second group of the receive devices via the second external memory bus (Column 45, lines 5 – 11). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Scheuneman's teaching of a high performance storage and include it in Runaldue's communication system in order to simultaneously move large amount of data or data frames (Column 2, lines 50 – 53).

Regarding claim 17, as part of Scheuneman's high performance memory there are a first and second multiplexers coupled to first and second groups of the receive devices (Figure 1a element 1a coupled to 2a, and 1b coupled to 2b and Column 5, lines 46 - 48), respectively, each of the first and second multiplexers being configured to receive the selection signals from the scheduler and to output a portion of a data frame.

Regarding claim 18, as part Scheuneman's high performance memory the switching device is further configured to alternately transfer data received from the first multiplexer to the first and second external memory buses and to alternately transfer data received from the second multiplexer to the first and second external memory

buses because as seen in figure 1a, the first device, 1a, goes through the multiplexer 2a and can send to any memory unit and the second device, 1b, goes through the multiplexer 2b and can travel to any storage unit, so the interface is configured to transfer data to the first or second memory unit for each device.

Claims 3, 7, 8, 12, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Runaldue in view of Scheuneman as applied to claims 1, 2, 4, 5, 6, 9, 10, 11, 13, 14, 15, 16, 17, and 18 above, and further in view of Springer (4,247,920).

Regarding claim 7, Runaldue discloses that the memory bus can operate at 100 MHz (Column 5, line 32), but Runaldue does not explicitly indicate that the buses can be each 8-bytes wide. Springer discloses an external memory, with 2 external memory buses (Figure 4, buses connected from element 128 to elements 122 and 124). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use 8 bits an a size for an external bus because of the design choice of the memory units, especially if the memory stores the capacity of 8 bit words (Column 3, lines 8 – 19)

Regarding claims 8 and 12, as part of Scheuneman's high performance storage the external memory interface includes a first external memory bus to transfer data to the first memory and a second external memory bus to transfer data to the second memory (Column 45, lines 5 – 11), but Scheuneman does not explicitly disclose that the external memory interface being further configured to generate odd address information when transferring data via the first external memory bus and even address information when transferring data via the second external memory bus. Springer teaches a

method of using 2 memories one being used for even memory storage and the other being odd memory storage (Column 4, lines 14 – 31). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use even and odd ranges as a deciding factor in which memory the device should access because this allows word accesses while using byte size memory (Column 1, lines 7 – 17).

Regarding claim 3, Scheuneman's high performance memory does not explicitly mention that the external memory interface is further configured to simultaneously transfer 8 bytes of data from the first receive device to the first memory and 8 bytes of data from the second receive device to the second memory. Springer discloses an external memory, configured to simultaneously transfer 8 bytes of data from the first receive device to the first memory and 8 bytes of data from the second receive device to the second memory (Figure 4, buses connected from element 128 to elements 122 and 124). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use 8 bits an a size for an external bus because of the design choice of the memory units, especially if the memory stores the capacity of 8 bit words (Column 3, lines 8 – 19)

Regarding claim 19, Scheuneman does not explicitly disclose that a first memory coupled to receive data frame information from the first external memory bus and configured to store data words having odd addresses; and a second memory coupled to receive data frame information from the second external memory bus and configured to store data words having even addresses. Springer teaches a method of using 2 memories one being used for even memory storage and the other being odd memory

storage (Column 4, lines 14 – 31). So Springer disclose a first memory coupled to receive data frame information from the first external memory bus and configured to store data words having odd addresses; and a second memory coupled to receive data frame information from the second external memory bus and configured to store data words having even addresses. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use even and odd ranges as a deciding factor in which memory the device should access because this allows word accesses while using byte size memory (Column 1, lines 7 – 17).

Regarding claim 20, as part as Springer's disclosure for using odd and even memories, he discloses the switching logic is configured to generate data address information having odd addresses for data transferred to the first memory and generate data address information having even addresses for data transferred to the second memory (Column 4, lines 14 – 31).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U. S. Patent No. 4,384,342 issued to Imura.

U. S. Patent No. 6,483,844 issued to Erimli.

U. S. Patent No. 5,887,148 issued to Lentz.

U. S. Patent No. 4,930,066 issued to Yokota.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Bates whose telephone number is (703) 605-0633. The examiner can normally be reached on 8 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hosain Alam can be reached on (703) 308-6662. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3800.

KB

KB
September 29, 2003

HOSAIN ALAM
SUPERVISORY PATENT EXAMINER